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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,667	12/28/2001	Seung-Kyu Choi	3430-0172P	3666

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EXAMINER

LANDAU, MATTHEW C

ART UNIT PAPER NUMBER

2815

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/028,667

Applicant(s)

CHOI ET AL.

Examiner

Matthew Landau

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2,5-9 and 11-22 is/are pending in the application.
- 4a) Of the above claim(s) 15-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-9,11-14 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

This application contains claim 15-21 drawn to an invention nonelected with traverse in the response filed April 19, 2003. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akamatsu et al. (US Pat. 6,414,730, hereinafter Akamatsu) in view of Han et al. (US Pat. 5,926,235, hereinafter Han).

In regards to claim 1, Figures 1 and 7A of Akamatsu disclose an array substrate for a liquid crystal display device, comprising: a substrate 51; gate and data lines (60 and 61) crossing each other on the substrate; a thin film transistor connected to the gate and data lines, the thin film transistor having a gate electrode 52, a semiconductor layer 54, and source and drain electrodes (58 and 59) facing and spaced apart from each other; a passivation layer 68 over the gate and data lines and the thin film transistor, the passivation layer having a contact hole exposing a portion of a side surface of the drain electrode; a gate insulation layer 53 formed

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underneath the passivation layer 68, wherein the contact hole is defined through the passivation layer and the gate insulation layer; and a pixel electrode 69 on the passivation layer. The difference between Akamatsu and the claimed invention is a storage capacitor including a portion of the gate line as a first storage electrode, a portion of a gate insulation layer, and a second storage electrode having an island shape, wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same electrode material as the source and drain electrodes. Figure 5I of Han discloses an array substrate with a thin film transistor and a storage capacitor. Figure 5I of Han discloses the storage capacitor includes a gate insulating film 109, a first storage electrode 117, and a second electrode 130, wherein the first storage electrode is formed of the same material as a gate electrode 107, and the second storage electrode is formed of the same material as a source and drain electrodes (105 and 106) (column 4, lines 1-22). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Akamatsu by including the storage capacitor of Han for the purpose of decreasing the response time of the pixels by allowing localized signal storage.

In regards to claim 2, Figure 7A of Akamatsu discloses the pixel electrode is electrically connected to the drain electrode through the contact hole, and also contact the substrate through the contact hole.

In regards to claim 5, Figure 7A of Akamatsu discloses the contact hole further exposes a portion of a top surface of the drain electrode.

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Claims 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han in view of Lyu.

In regards to claims 6 and 8, Figures 4 and 6B of Han disclose a substrate 110; gate and data lines (117 and 115) crossing each other on the substrate; a thin film transistor having a gate electrode 107 extending from the gate line, a semiconductor layer 111, first and second ohmic contact layers 112, and source and drain electrodes (105 and 106), a passivation layer 113a pattern on the data line and the thin film transistor, the passivation layer pattern exposing a portion of a side surface of the drain electrode; and a pixel electrode 104 connected to the drain electrode; and a gate insulation film 109 formed directly on the gate insulation film at a pixel region defined by the gate and data lines. It is considered that the slanted portion of the drain electrode 106 is "a side surface", since it is a side of the upper portion of the drain electrode. The difference between Han and the claimed invention is the semiconductor layer and the ohmic contact layers having ends aligned with and directly below corresponding ends of the source electrode and drain electrodes. Figure 3I of Lyu discloses a thin film transistor with a semiconductor layer 137 and ohmic contact layers 139 having ends aligned with and directly below the corresponding ends of the source and drain electrodes. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Han by using the layer alignment of Lyu for the purpose of simplifying the production process and reducing manufacturing costs.

In regards to claim 7, Figures 4 and 6B of Han disclose a storage capacitor including a first storage electrode 117, a portion of a gate insulation layer 109, and a second storage electrode 130, wherein the first storage electrode is formed of the same material as the gate

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electrode and the second storage electrode is formed of the same material as the source and drain electrode (col. 4, lines 1-22), and wherein the pixel electrode 104 contacts the second storage electrode through a contact hole formed through the passivation layer.

In regards to claim 9, Figure 6B of Han discloses the passivation layer pattern exposes a portion of only one side surface of the drain electrode.

In regards to claim 11, Figure 6B of Han discloses the passivation layer 113a pattern further exposes a portion of a top surface of the drain electrode.

Claims 12-14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lyu.

In regards to claim 12, Figures 4 and 8 of Kim disclose an array substrate for a liquid crystal display device, comprising: a substrate 100; a gate line 130a on the substrate; a gate insulator 120 on the gate line; a semiconductor layer 110 on the gate insulator; a first ohmic contact layer and a second ohmic contact layer (para. [0037]) on the semiconductor layer; a data line 150 and source and drain electrodes (150 and 170) on the plurality of ohmic contact layers, the source electrode connected to the data line, the drain electrode facing and spaced apart from the source electrode; a passivation layer 160 on the source and drain electrodes and covering a crossing portion of the gate and data lines, a portion of a side surface of the drain electrodes being exposed; a pixel electrode 7 connected to the drain electrodes; wherein the gate insulator comprises a gate insulation film 120 formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film at a pixel region defined by the gate and data lines. Note that Kim discloses in paragraph [0037] that the source and drain electrodes are

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in ohmic contact with the respective source and drain regions of the active layer 110, therefore it is considered that these source and drain regions are the ohmic contact layers. The difference between Kim and the claimed invention is the semiconductor layer and the ohmic contact layers having ends aligned with and directly below corresponding ends of the source electrode and drain electrodes. Figure 3I of Lyu discloses a thin film transistor with a semiconductor layer 137 and ohmic contact layers 139 having ends aligned with and directly below the corresponding ends of the source and drain electrodes. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kim by using the layer alignment of Lyu for the purpose of simplifying the production process and reducing manufacturing costs.

In regards to claim 13, Figure 8 of Kim discloses a portion of the pixel electrode is formed directly on the gate insulator.

In regards to claim 14, Figure 8 of Kim discloses the passivation layer patter 160 further exposes a portion of a top surface of the drain electrode 170.

In regards to claim 22, Figure 8 of Kim discloses a storage capacitor including a first storage electrode 130b, a portion of the gate insulator 120, and a second storage electrode 170, wherein the pixel electrode 7 contacts the second storage electrode through a contact hole formed through the passivation layer, and wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same material as the source and drain electrodes (paragraphs [0036] and [0037]).

*Response to Arguments*

Applicant's arguments filed July 13, 2004 have been fully considered but they are not persuasive.

Applicant argues that the Examiner has not demonstrated a proper motivation to combine Akamatsu with Han because Akamatsu already discloses localized signal storage. Applicant refers to Figure 12 of Akamatsu, which shows a capacitor in each pixel. However, it is respectfully pointed out that Figure 12 shows a conventional active matrix configuration and is not the invention of Akamatsu (col. 1, lines 19-35 and col. 7, lines 39-42). Applicant further argues that the Examiner's cited motivation "is nothing more than a broad conclusory statement about both Akamatsu and Han, and does not constitute evidence of proper motivation to provide the storage capacitor features of Han for Akamatsu". The provided motivation clearly recites a specific advantage/improvement resulting from the proposed combination and is therefore not a "broad conclusory statement". Having storage capacitors in LCD pixels to increase switching speeds/decrease response time is extremely common and well known in the art. Therefore, motivation provided in the above rejection is proper and Applicant's arguments are not persuasive.

In response to Applicant's arguments regarding Han in view of Lyu that the "alleged motivation is not supported by objective evidence of record and is improperly based solely on speculation unsupported by objective evidence or record", although Lyu may not explicitly disclose a reason for having the claimed configuration, it is very well known in the art that having the ends aligned as claimed means the device can be made with fewer masking steps. Therefore, the production process would be simplified as stated in the above rejection. It is



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noted that the motivation to combine references does not necessarily have to come from the references themselves, but instead can be drawn from the knowledge of persons of ordinary skill in the art. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Note that Applicant makes similar arguments against the rejection of Kim in view of Lyu.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

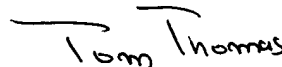
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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Matthew C. Landau

Examiner

November 1, 2004